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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/758,317	01/15/2004	Vincent S. Chang	2003-0287/24061.627	5370

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EXAMINER	
DEO, DUY VU NGUYEN	
ART UNIT	**PAPER NUMBER**
1765	

DATE MAILED: 09/26/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/758,317	CHANG ET AL.	
	Examiner	Art Unit	
	DuyVu n. Deo	1765	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 January 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *15 January 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *3/29/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-5, 17, 18 are rejected under 35 U.S.C. 102(e) as being anticipated by Yamaguchi (US 2003/0232491).

Yamaguchi describes a method for forming MOSFET comprising: forming a gate insulator silicon oxide on the substrate (paragraph [0041]); forming a nitrided gate insulator (paragraphs [0042-0045, 0061-0065]); performing a thermal processing (claimed anneal procedure) (paragraphs [0049-0051]); forming a conductive gate structure on a portion of the nitrided gate insulator (paragraphs [0052,0053]); forming a LLD source/drain regions on the substrate using he gate electrode structure as the mask (claimed forming LLD source/drain regions in the area of the substrate not covered by the conductive gate structure) (paragraph [0053]); forming sidewall insulator spacers on the side of the gate structure (paragraph [0054]); forming a heavily doped source/drain regions in the area not covered by the gate structure and the sidewall spacers (paragraph [0055]).

Referring to claims 2, 3 and 18, the silicon oxide gate insulator is formed by thermal oxidation at a thickness of 10 angstrom (paragraph [0041]) and nitrided silicon dioxide layer would have an equivalent oxide thickness of about 10 angstrom.

Referring to claim 4, the nitride silicon dioxide layer would have a dielectric constant between 3.9-7.8.

Referring to claim 5, the nitrided gate insulator layer is formed by plasma nitridation procedure at 50-3000 Watts using N2 and He (paragraph [0064]).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 6-16, 19, 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamaguchi as applied to claims 1 above, and further in view of Shih et al. (US 6,387,761).

Referring to claim 6, Yamaguchi doesn't describe forming the nitrided gate insulator layer by annealing process at T 600-1100 degrees C in either NH3, NO, or N2O. Shih teaches that nitrided gate insulator can be formed either by a plasma process or a thermal nitridation (claimed annealing) at T 800-950 degree C in NH3 (col. 4, line 5-27). At the time of the invention, one skilled in the art, in light of Shih, would find it obvious to use either process to from the nitride gate insulator layer with a reasonable expectation of success.

Referring to claims 7-9, 19, 20 Yamaguchi doesn't describe the annealing process comprises hydrogen. Shih teaches the annealing process is done in N2/H2 gases (col. 4, line 29-67). It would have been obvious for one skilled in the art to modify Yamaguchi's annealing process by adding H2 because Shih teaches that annealing in N2/H2 would eliminate defects

such as pinholes in silicon nitride and cure defects such as dangling bonds at the silicon nitride/polysilicon electrode surface to form a high quality interface between silicon nitride and polysilicon electrode. The annealing T is 700-850 degrees C, with a H2 concentration including 10 % and the annealing time is 60-180 seconds (col. 4, line 53-67).

Unlike claimed invention, applied prior art above doesn't describe the anneal procedure is performed in the same tool to be used for deposition of the conductive gate material. However, one skilled in the art at the time of the invention would find it obvious to perform different procedures including the annealing and deposition procedure in the same tool because it would eliminate the down time of transferring substrate to different tools that would reduce production yield and it also eliminate the contamination of the substrate when moving from one tool to the other.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to DuyVu n. Deo whose telephone number is 571-272-1462. The examiner can normally be reached on 6:00-2:30 Mon-Fri.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nadine Norton can be reached on 571-272-1465. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Primary Examiner
Duy-Vu N. Deo
9/19/05